REMARKS

In response to the Office Action dated January 13, 2003, claims 1, 10 and 17 have been amended. Claims 1-20 remain in the case. Reexamination and reconsideration of the application, as amended, are requested.

The Office Action rejected claims 1-20 under 35 U.S.C. § 112, first paragraph for allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Also, the Office Action rejected claims 1-20 under 35 U.S.C. § 112, second paragraph as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Record is made of a telephonic interview between Applicants' attorney Edmond A. DeFrank and Examiner Judy Nguyen on April 2, 2003. The specification, drawings and pending claims were discussed. A proposed amendment modifying the drawings, specification and independent claims 1, 10 and 17 were discussed during the interview. Although an agreement was not reached regarding the allowability of the claims, the Examiner suggested clarification changes to claims 1, 10 and 17, the specification on pages 7-8, as well as FIG. 4.

Although the Applicants contend that the specification, drawings and claims comply with 35 U.S.C. § 112, first paragraph and 35 U.S.C. § 112, second paragraph before the amendments, in an effort to expedite the prosecution of this case, the Applicants have amended the specification and claims 1, 10 and 17 as suggested by the Examiner in the above mentioned interview. The Applicants submit that no new matter has been added to the claims or the specification.

In addition, the Applicants submit herewith a new proposed drawing, as suggested by the Examiner during the interview. Namely, FIG. 4B has been added to clarify the invention. The Applicants submit that no new matter has been added.

In view of the arguments and amendments set forth above, the Applicants respectfully submit that the claims of the subject application are in immediate condition for allowance. The Examiner is respectfully requested to withdraw the outstanding claims rejections and to pass this application to issue. Additionally, in an effort to expedite and further the prosecution of the subject application, the Applicants kindly invite the Examiner to telephone the Applicants' attorney at (818)

885-1575 if the Examiner has any questions or concerns. Please note that all correspondence should continue to be directed to:

Hewlett Packard Company
Intellectual Property Administration
P.O. Box 272400
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Respectfully submitted,
Dated: April 14, 2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The following are marked-up versions of the first full paragraph on page 4 (lines 1-2):

FIG. 4A shows one embodiment for illustrative purposes a cross section of the thin film circuitry.

The following are marked-up versions of the third full paragraph on page 7 (lines 26-31) and continuing to the first partial paragraph of page 8 (lines 1-7):

FIG. 4A illustrates a cross section of a portion of the printhead 100 of FIG. 1 in one embodiment, for illustrative purposes only. FIG. 4B is a block diagram showing the embodiment of FIG. 4A. The layers of FIG. 4A are presented as an illustration and are not to scale. Referring to FIG. 1 and FIG. 2 along with FIGS. 4A and 4B, in one embodiment, the primitives 1-n 108, 110 are made of thin films [circuitry] and include an orifice plate 315 with nozzles 318 mounted on a barrier 375 that is coupled to a thin film circuit 401. Also included is a metal stack 403 comprised of a first metal layer 402 and a second metal layer 404. The first metal layer 402 can be Aluminum Copper Silicon. The second metal layer 404 [is conformed with] includes plural power vias 406 (FIG. 4A illustrates one power via 406 and one resistor 112 for illustrative purposes only) and includes a top conductive metal 400, which can be Aluminum, and a bottom metal barrier 407[,], which can be Tantalum Aluminum. [which at one portion is the r]Resistor 112 is defined by a portion of the top conductive metal 400 and the bottom metal barrier 407. [and at another portion is a] The separation barrier 408 is defined by a bottom portion of the power via 406 that is adjacent to the first metal layer 402. Also, other layers 411 are included, but are not described here for simplicity.

The following are marked-up version of the second full paragraph on page 8 (lines 8-17):

The power vias 406 form an interface between the first metal layer 402 and the second metal layer 404 for providing power and control to the resistors 112. Also, the power vias 406 form a blockade between the second metal layer 404 and a substrate 409. The substrate 409 could be tetraethylorthosilicate (TEOS) or some such other compound. The [predefined vias 406 form the] separation barriers 408 of the respective power vias 406 are formed between conductive portions of [a] the thin film

resistor 112 and an associated power source 430, which derives power from the power bus 128 of FIG. 1. The separation barrier 408 is preferably made of a non-corrosive material, such as Tantalum Aluminum, Tungsten Silicon Nitride, or Tantalum Nitride. As a result, the electrical properties of the circuit are minimally affected while decreasing the possibility of an electrical open.

IN THE CLAIMS

The following are marked-up versions of amended claims 1, 10 and 17:

1. (Once Amended) A printhead having a circuit with plural resistors and a power [bus] source, comprising:

a metal stack formed within the circuit and comprised of a first metal layer coupled to the power source and a second metal layer having a portion that forms the resistors; and

at least one power via formed within the circuit as an interface between the first metal layer and the second metal layer, the power via including [and as] a separation barrier located adjacent the first metal layer and between the resistors and the power [bus] source.

10. (Once Amended) In an ink jet printhead, a method for increasing resistance to ink corrosion of a thin film circuit[,] having a portion defined by at least one thin film resistor, the method comprising:

connecting a power source to the thin film resistor with a power via; and

[separating a thin film resistor from a power bus in the thin film circuit] substantially preventing spreading of the ink corrosion from the thin film resistor to a power source with a separation barrier portion of the power via[; and

protecting the power bus from ink exposure].

17. (Once Amended) A method of manufacturing a circuit for an ink jet printhead, the circuit having plural resistors, a power bus and a controller bus, the method comprising:

[routing] creating [a] conductive trace routes from the power bus to power vias associated with each resistor and to each resistor and from the controller bus to controller vias associated with each resistor and to each resistor; and

[protecting the power bus from ink penetration with the power vias for increasing resistance to corrosion]

creating a separation barrier within the power via to substantially prevent spreading of the ink corrosion from the resistors to the power bus and the controller bus.